FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200301825-5	10/693,388	

APPLICANT	
Luiz Andre Barroso et al.	
FILING DATE	GROUP
10-24-2003	2186

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
M	1A	5,386,547	01-31-95	Jouppi	
	1B	5,778,437	07-07-98	Baylor et al.	
	1C	6,295,598	09-25-01	Beroni et al.	
	1D	6,202,127	03-13-01	Dean et al.	
	1E	5,457,679	10-10-95	Eng et al.	
	1F	5,440,752	08-08-95	Lentz et al.	
	1G	6,457,100	09-24-02	Ignatowski et al.	
	1H	6,263,405	07-17-01	Irie et al.	
	1I	5,634,110	05-27-97	Laudon et al.	
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

M	1Q	Agrawal, Anant, et al., "An Evaluation of Directory Schemes for Cache Coherence", Proceedings of 15th International Symposium on Computer Architecture ("ISCA") (May 1998) pp. 280-289
M	1R	Barroso, Luiz Andre, et al., "Impact of Chip-Level Integration on Performance of OLTP Workloads", High-Performance Computer Architecture ("HPCA") (January 2000)
M	1S	Barroso, Luiz Andre, et al., "Memory System Characterization of Commercial Workloads", ISCA (June 1998)

EXAMINER	DATE CONSIDERED
Thuy Li.	August 5, 04

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N	2Q	Eggers, Susan J., et al., "Simulation Multithreading: A Platform for Next-generation Processors", University of Washington, DEC Western Research Laboratory ((eggers.levyjlo)@cs.washington.edu) ((emer.stamm)@vssad.enet.dec.com) pp. 1-15
N	2R	Eickemeyer, Richard J., et al., "Evaluation of Multithreaded Uniprocessors for Commercial Application Environments", ACM (1996) (0-89791-786-3) pp. 203-213
N	2S	Gupta, Anoop, et al., "Reducing Memory and Traffic Requirements for Scalable Directory-Based Cache Coherence Schemes", Stanford University, Computer Systems Laboratory, pp 1-10

EXAMINER	DATE CONSIDERED
Duo Li.	08/05/04

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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

✓	3Q	Hammond, Lance, et al., "A Single-Chip Multiprocessor", IEEE (September 1997) (0018-9162)
✓	3R	Hammond, Lance, et al., "Data Speculation Support for a Chip Multiprocessor", Stanford University, Computer Systems Laboratory (http://www.hydra.stanford.edu/)
✓	3S	Jouppi, Norman P., et al., "Tradeoffs in Two-Level On-Chip Caching", WRL Research Report 93/3, Western Research Laboratory (WRL-Techreports@decwri.dec.com) (December 1993) pp. 1-31

EXAMINER	DATE CONSIDERED
Thuo Li.	08/06/06

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✓	4Q	Krishnan, Venkata, et al., "Hardware and Software Support for Speculative Execution of Sequential Binaries on a Chip-Multiprocessor", University of Illinois at Urbana-Champaign (http://iacoma.cs.uiuc.edu)
✓	4R	Kuskin, Jeffrey, et al., "The Stanford FLASH Multiprocessor", Stanford University, Computer Systems Laboratory
✓	4S	Laudon, James, et al., "The SGI Origin: A ccNUMA Highly Scalable Server", Silicon Graphics, Inc. (laudon@sgi.com)

EXAMINER	Zhuo Li.	DATE CONSIDERED	08/06/04

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✓	5Q	Lenoski, Daniel et al., "The Directory-Based Cache Coherence Protcol for the DASH Multiprocessor", IEEE (1990) (CH2887-8) pp. 148-159
✓	5R	Nayfeh, Basem A., et al., "Evaluation of Design Alternatives for a Multiprocessor Microprocessor", ACM (1996) (0-89791-786-3) pp. 67-77
✓	5S	Nowatzyk, Andreas G., et al., "S-Connect: from Networks of Workstations to Supercomputer Performance", 22nd Annual International Symposium on Computer Architecture ("ISCA") (June 1995)

EXAMINER	DATE CONSIDERED
Zhuo Li	08/06/04

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✓	6Q	Nowatzyk, Andreas, et al., "Exploiting Parallelism in Cache Coherency Protocol Engines", Sun Microsystems Computer Corporation
✓	6R	Olukotun, Kunle, et al., "The Case of a Single-Chip Multiprocessor", Proceedings Seventh International Symposium Architectural Support for Programming Languages and Operating Systems ("ASPLOS VII") (October 1996)
✓	6S	Steffan, J. Gregory, et al., "The Potential for Using Thread-Level Data Speculation to Facilitate Automatic Parallelization", HPCA-4 (February 1998) pp. 1-12

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✓	7Q	Tremblay, Marc, "MAJC-TM-5200 AVLIW Convergent MPSOC", Sun Microsystems, Inc., Microprocessor Forum (1999)
✓	7R	Kunkel, Steven, et al., "System Optimization for OLTP Workloads, IEEE (1999) (0272-1732) pp. 56-64
✓	7S	Diefendorff, Keith, "Power4 Focuses on Memory Bandwidth", Microdesign Resources, Microprocessor Report vol 13 No. 13, October 6, 1999

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Zhuo Li	08/06/04